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(54) **PIXEL SENSING DEVICE AND ORGANIC LIGHT EMITTING DISPLAY DEVICE INCLUDING THE SAME**

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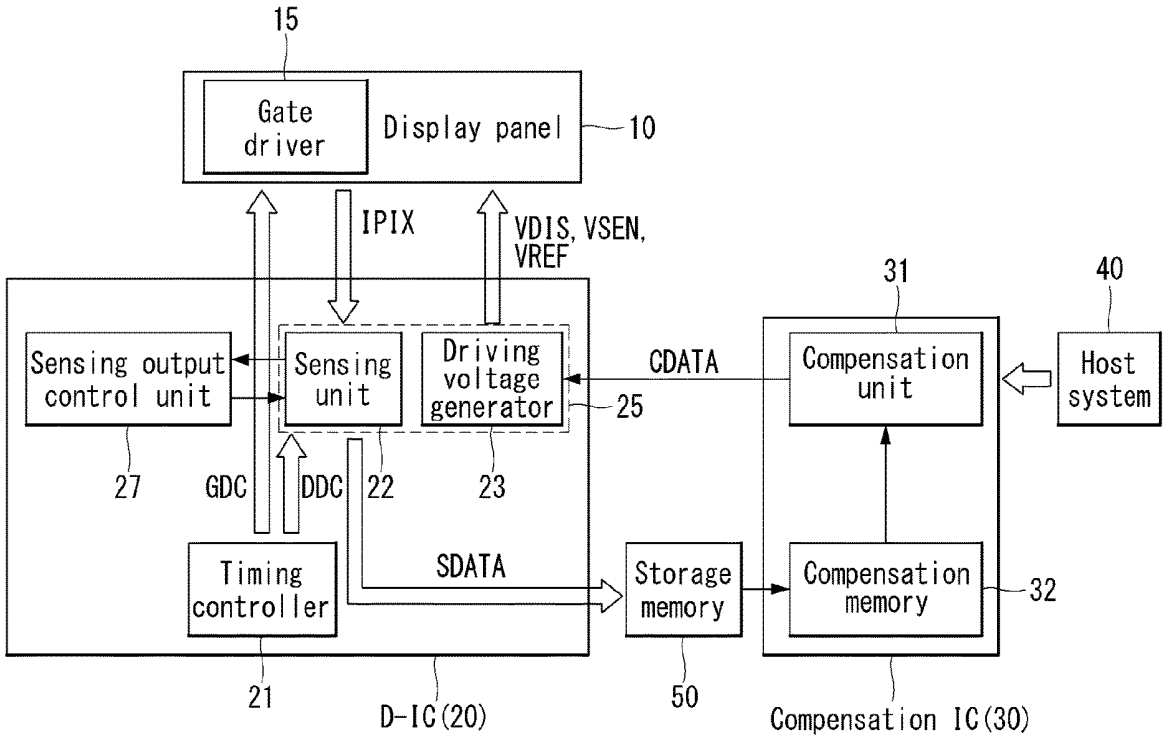
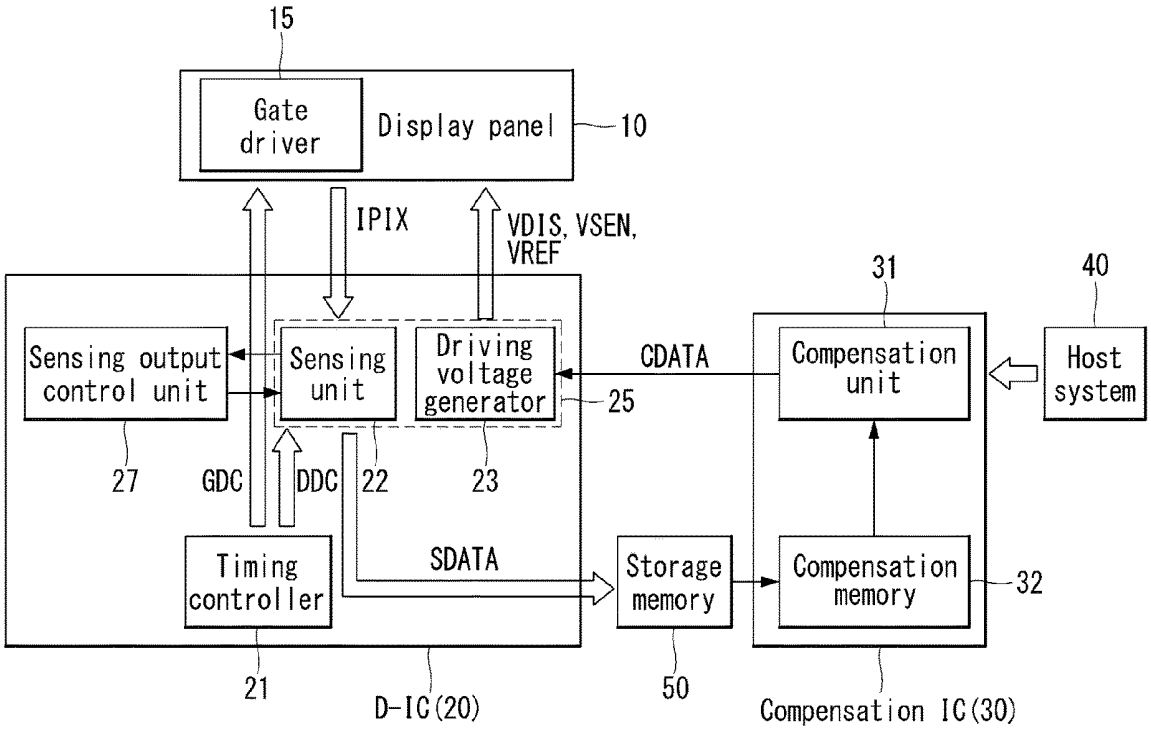
(57) **ABSTRACT**

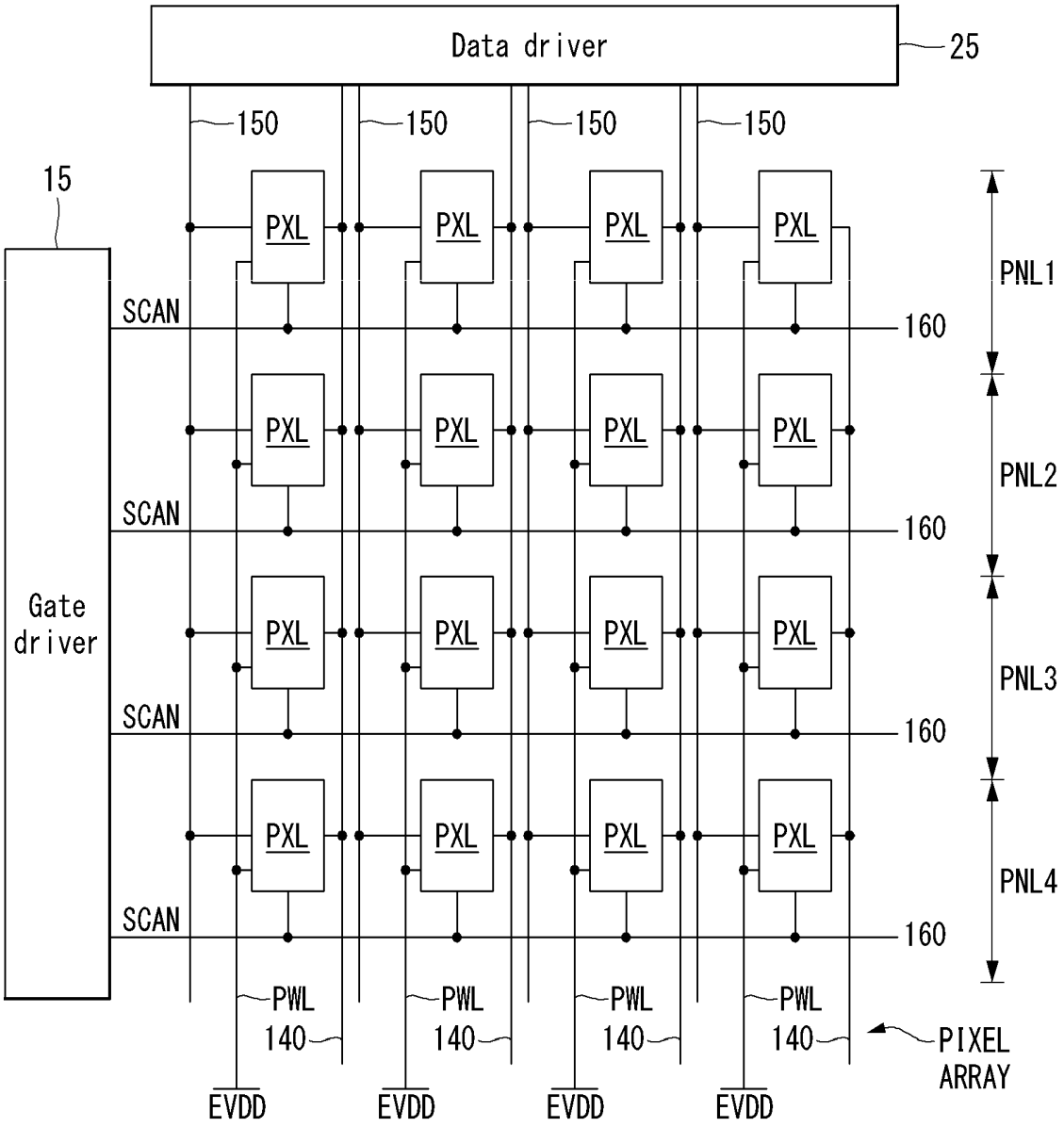
The present disclosure relates to a pixel sensing device and the organic light emitting display device including the same which reduce or minimize the influence of the panel noise and improve sensing accuracy and sensing reliability. The pixel sensing device includes a current integrator connected to a pixel through a sensing line of a display panel and integrating a pixel current flowing through the pixel to generate an integrator output voltage; a sample and hold unit sampling and holding the integrator output voltage; an analog to digital converter (ADC) converting the integrator output voltage output from the sample and hold unit into a digital signal; and a first capacitor serving to reduce or minimize a distortion degree of the integrator output voltage due to panel noise mixed to the pixel current.



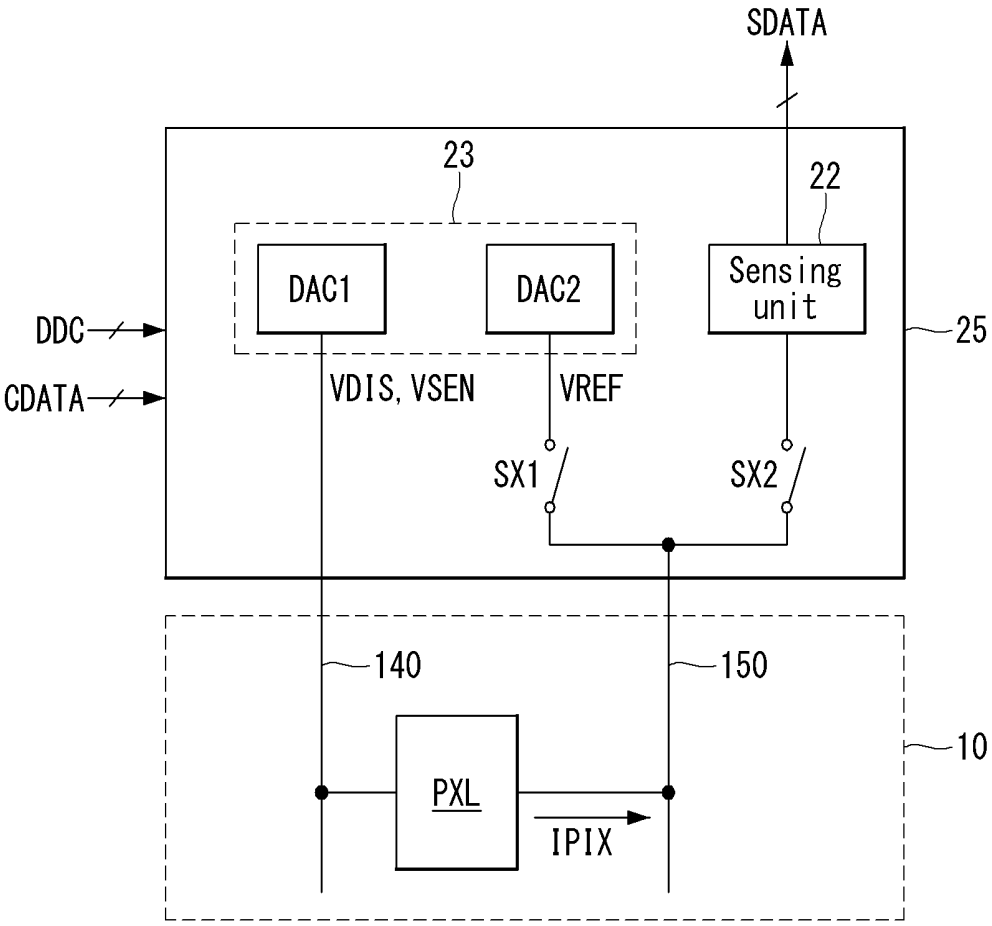
# FIG. 1


15
Gate driver
Display panel
10
IPIX
VDIS, VSEN, VREF
31
40
Sensing output control unit
Sensing unit
Driving voltage generator
CDATA
Compensation unit
Host system
25
27
GDC
DDC
22
23
Timing controller
SDATA
Storage memory
Compensation memory
32
21
D-IC(20)
50
Compensation IC(30)

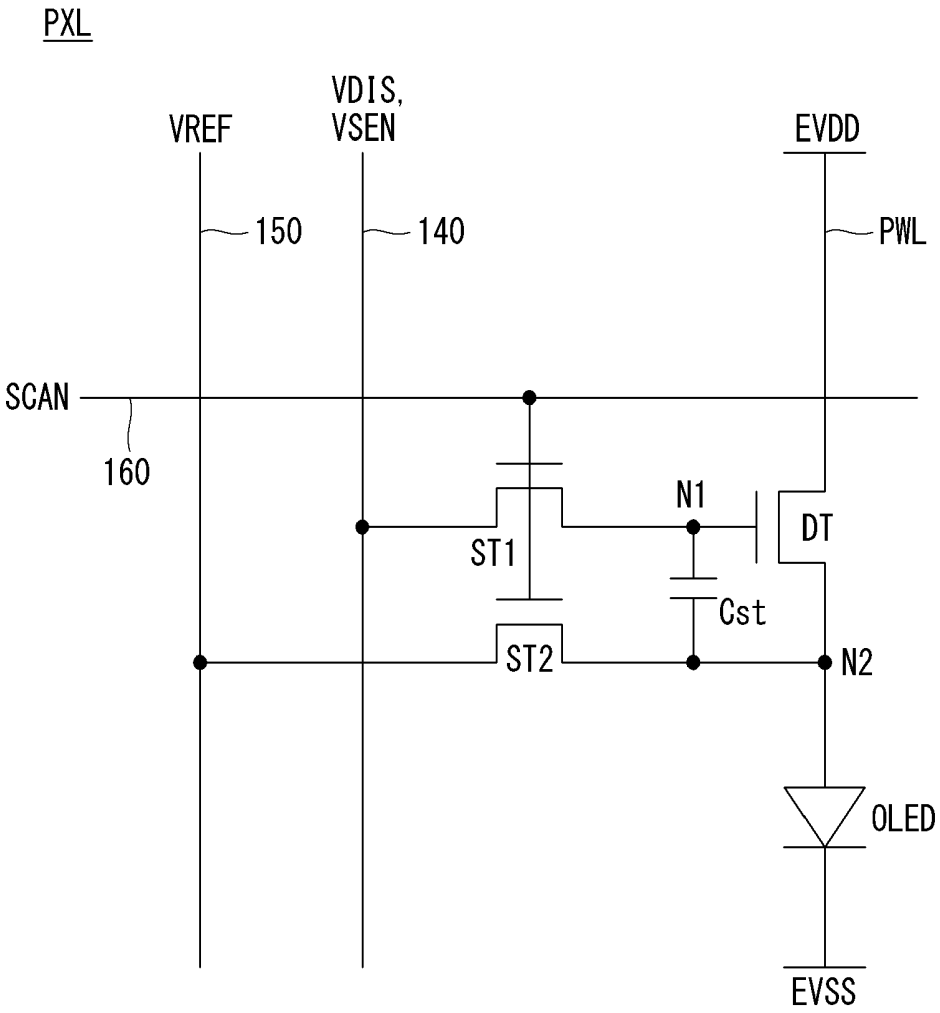
# FIG. 2


Data driver
25
150
150
150
150
15
PXL
SCAN
160
PNL1
PNL2
PNL3
PNL4
Gate driver
PWL
140
EVDD
PIXEL ARRAY

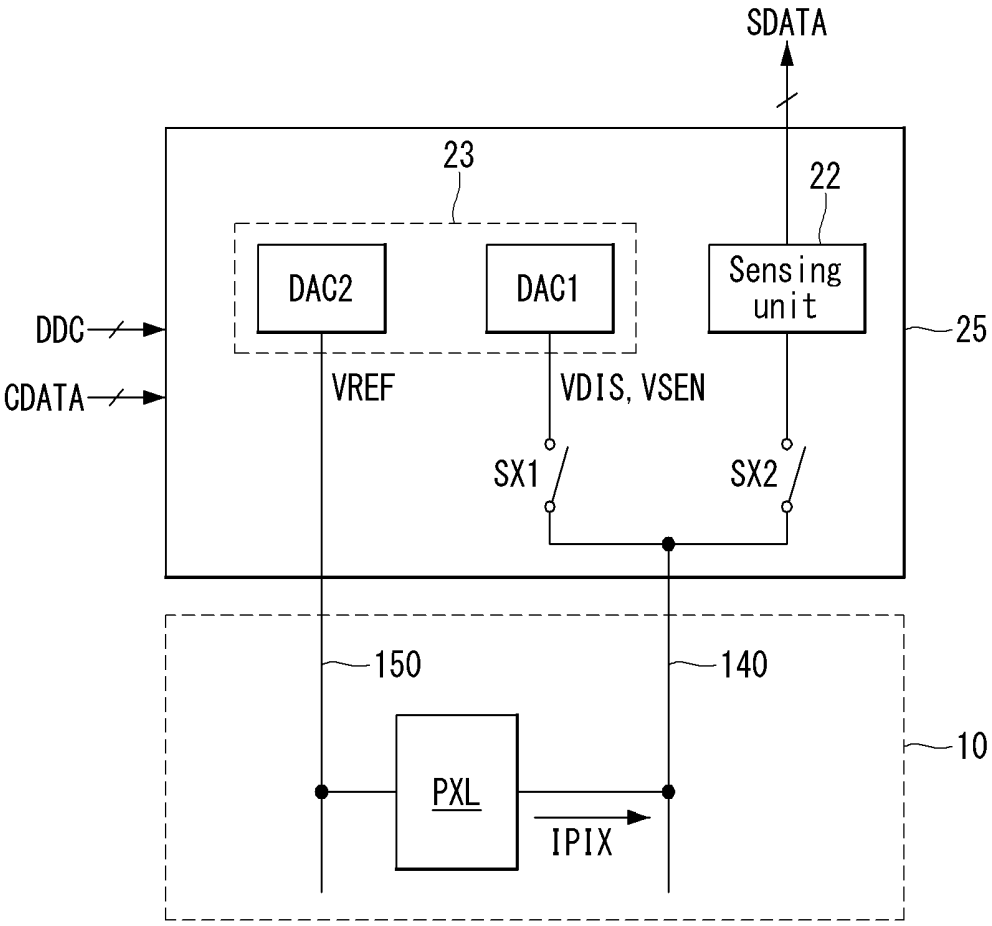
# FIG. 3


SDATA
23
22
DAC1
DAC2
Sensing unit
25
DDC
CDATA
VDIS, VSEN
VREF
SX1
SX2
140
150
10
PXL
IPIX

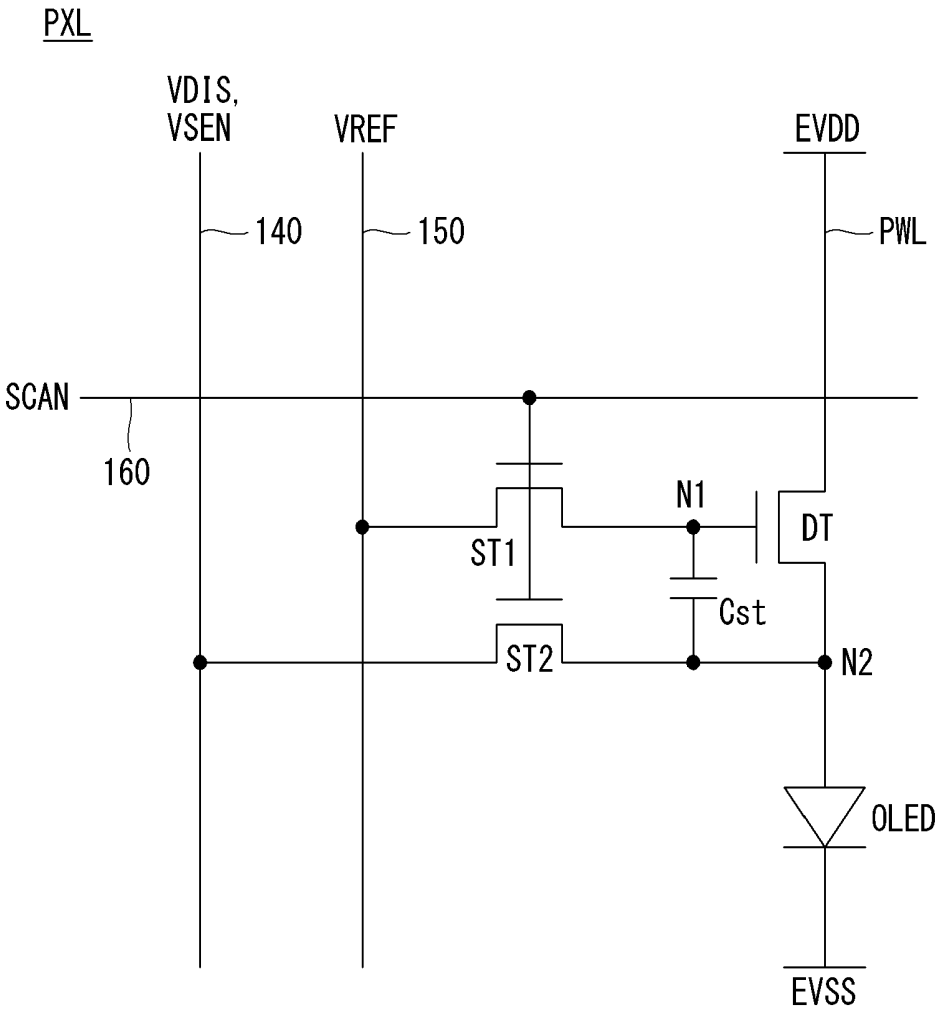
# FIG. 4


PXL
VDIS,
VSEN
VREF
EVDD
150
140
PWL
SCAN
160
N1
DT
ST1
Cst
ST2
N2
OLED
EVSS

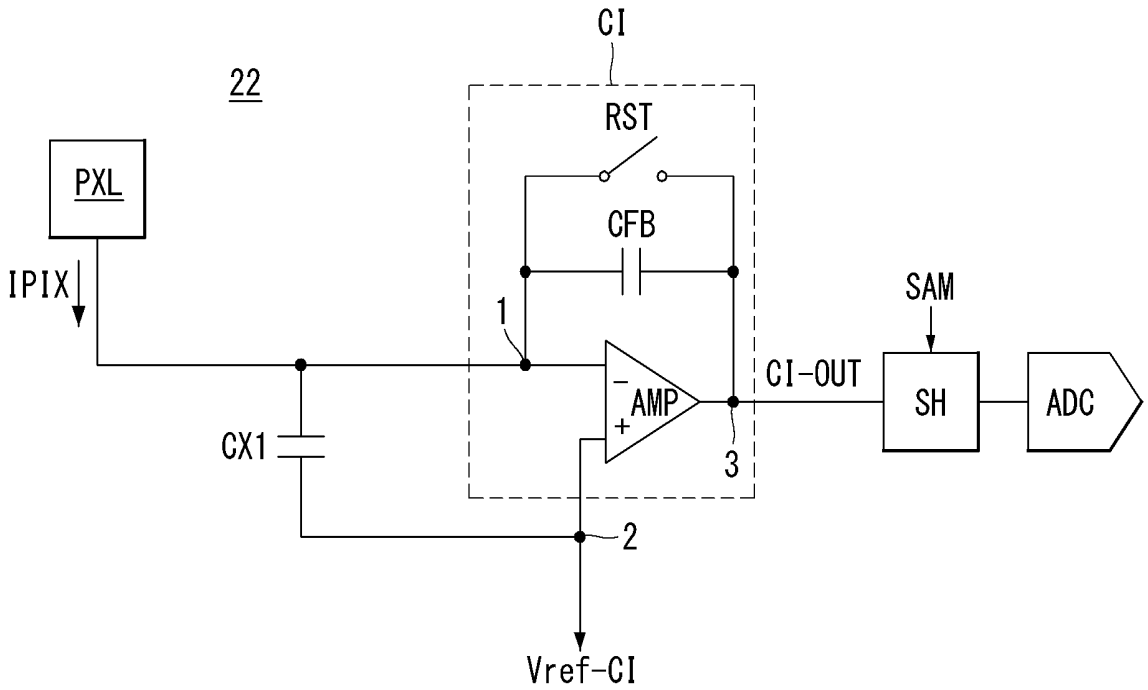
# FIG. 5


SDATA
23
22
DAC2
DAC1
Sensing unit
DDC
CDATA
25
VREF
VDIS, VSEN
SX1
SX2
150
140
10
PXL
IPIX

# FIG. 6


PXL
VDIS,
VSEN
VREF
EVDD
140
150
PWL
SCAN
160
N1
DT
ST1
Cst
ST2
N2
OLED
EVSS

# FIG. 7



# FIG. 8

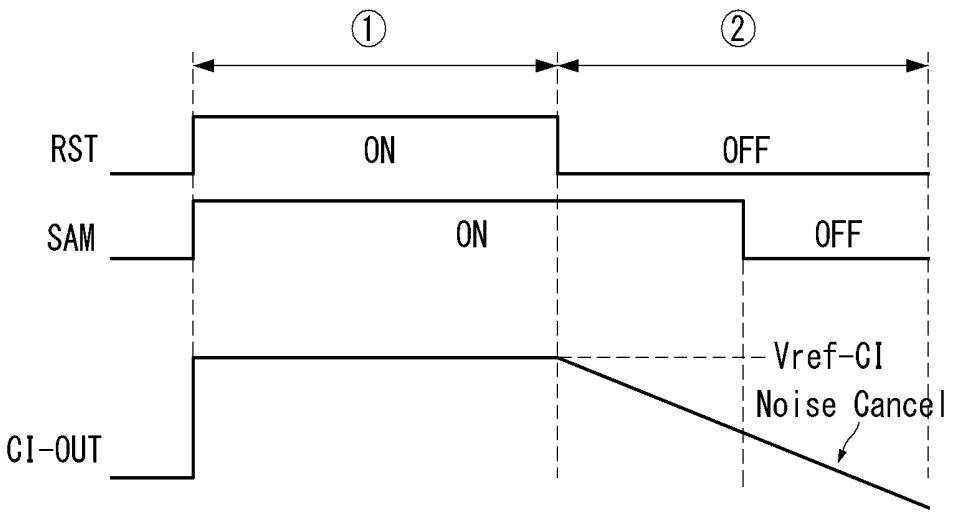


FIG. 9

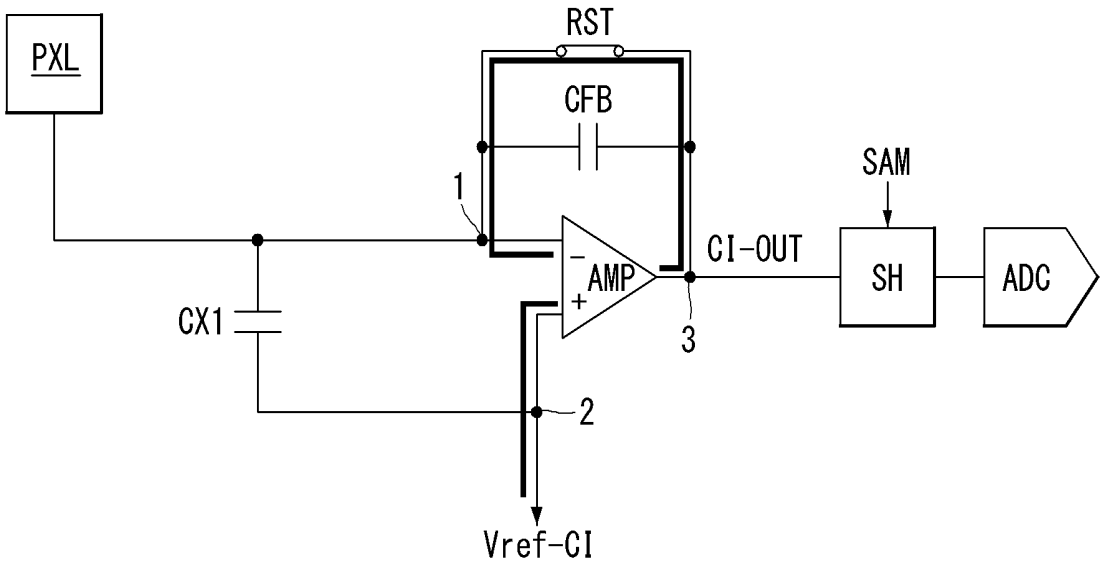
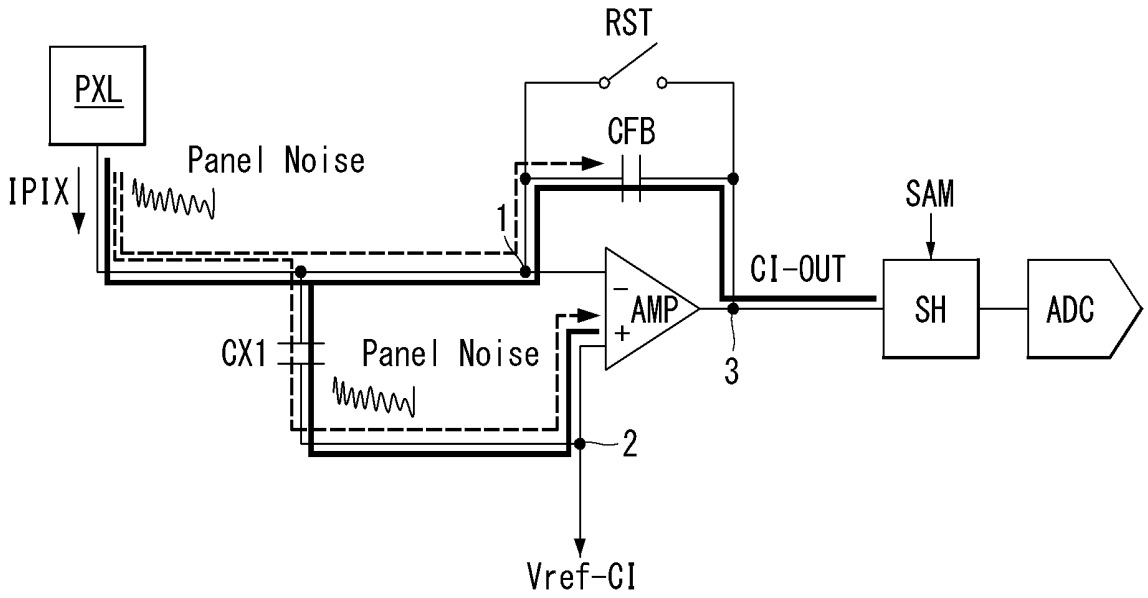
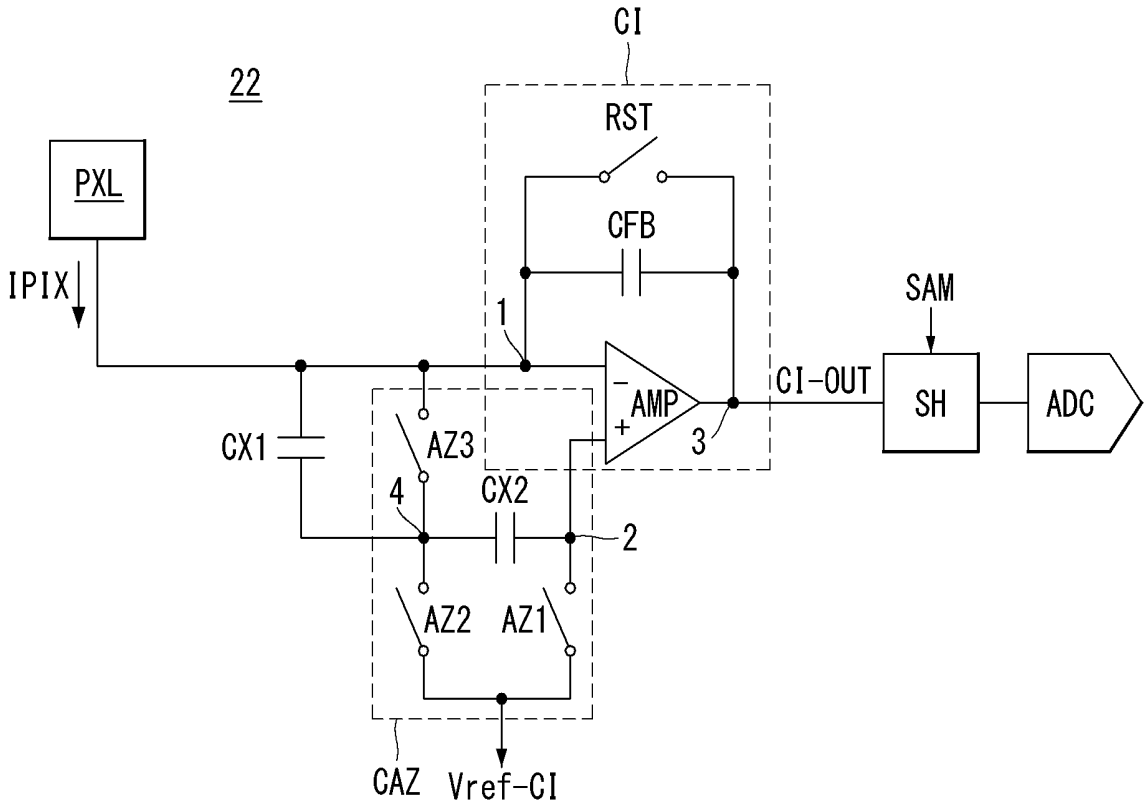

PXL
RST
CFB
SAM
1
CI-OUT
AMP
SH
ADC
CX1
3
2
Vref-CI

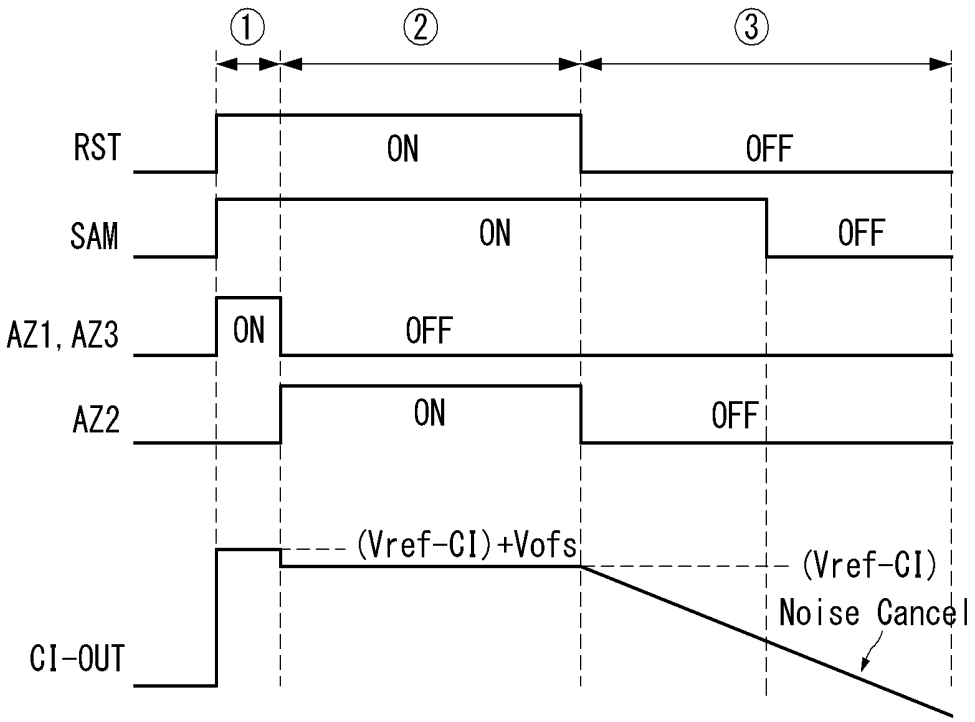
FIG. 10


RST
PXL
CFB
Panel Noise
IPIX
SAM
1
CI-OUT
AMP
SH
ADC
CX1
Panel Noise
3
2
Vref-CI

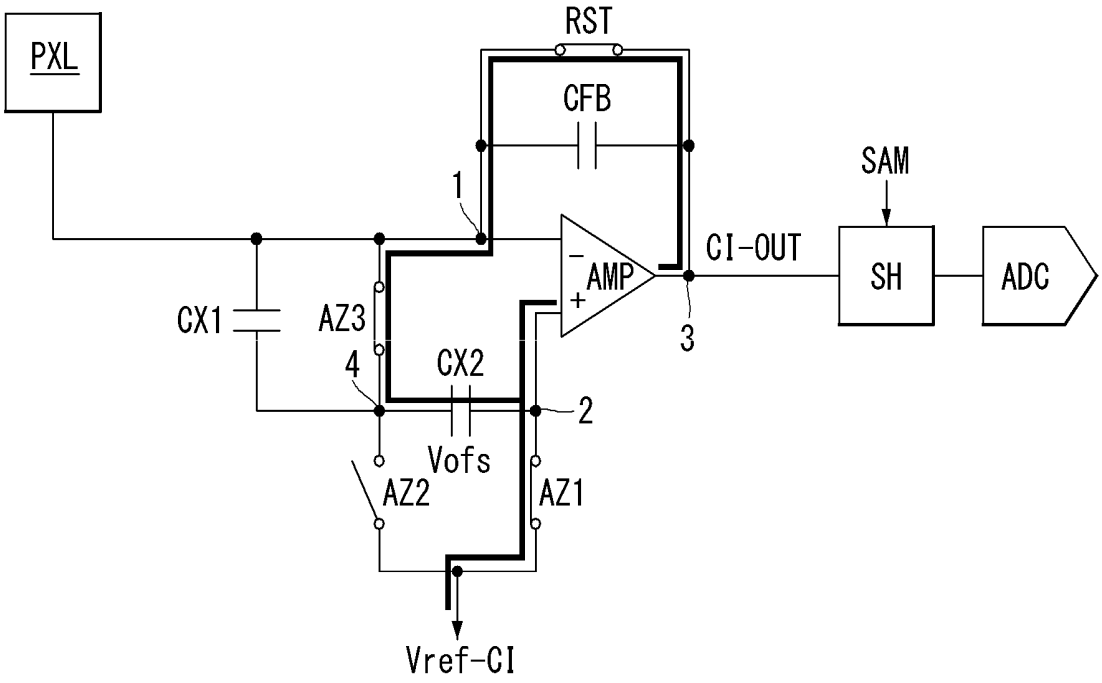
# FIG. 11


CI
22
RST
PXL
CFB
IPIX
SAM
1
AMP
CI-OUT
SH
ADC
CX1
AZ3
3
4
CX2
2
AZ2
AZ1
CAZ
Vref-CI

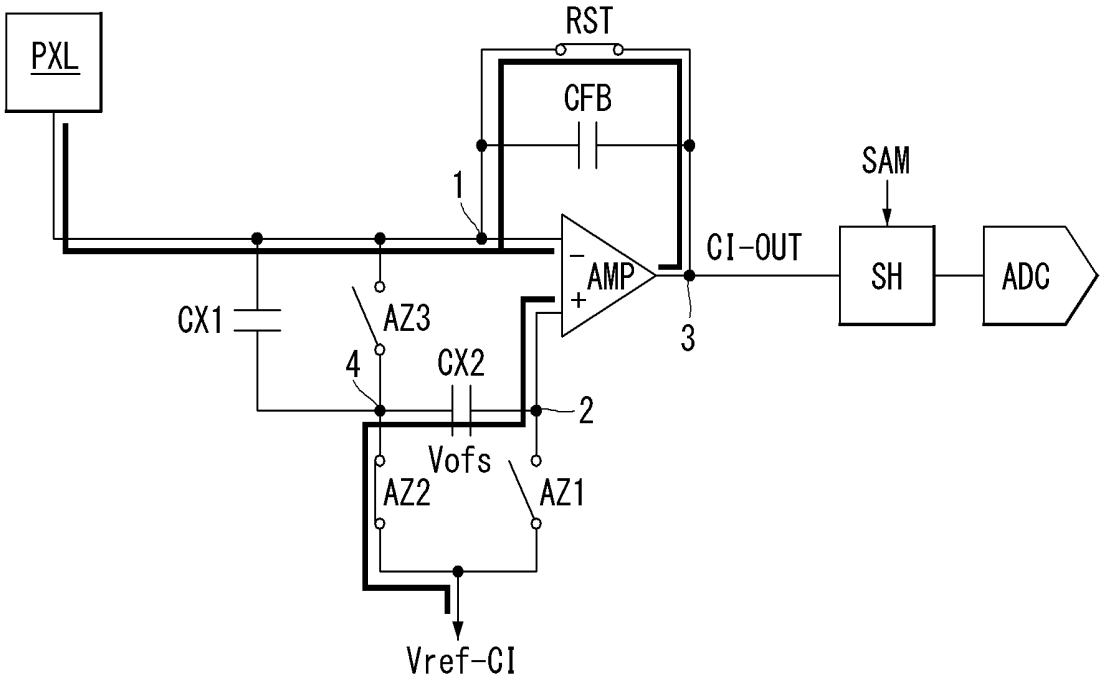
# FIG. 12


①
②
③
RST
ON
OFF
SAM
ON
OFF
AZ1, AZ3
ON
OFF
AZ2
ON
OFF
(Vref-CI)+Vofs
(Vref-CI)
Noise Cancel
CI-OUT

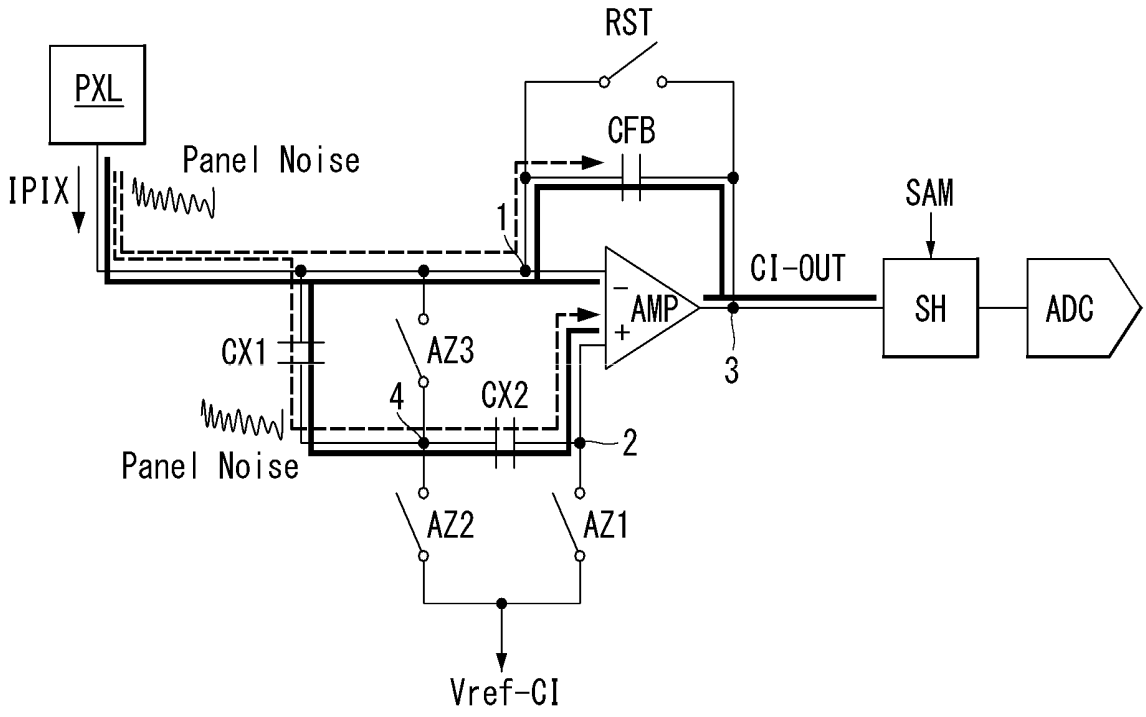
# FIG. 13


PXL
RST
CFB
SAM
1
CI-OUT
AMP
SH
ADC
CX1
AZ3
4
CX2
3
2
Vofs
AZ2
AZ1
Vref-CI

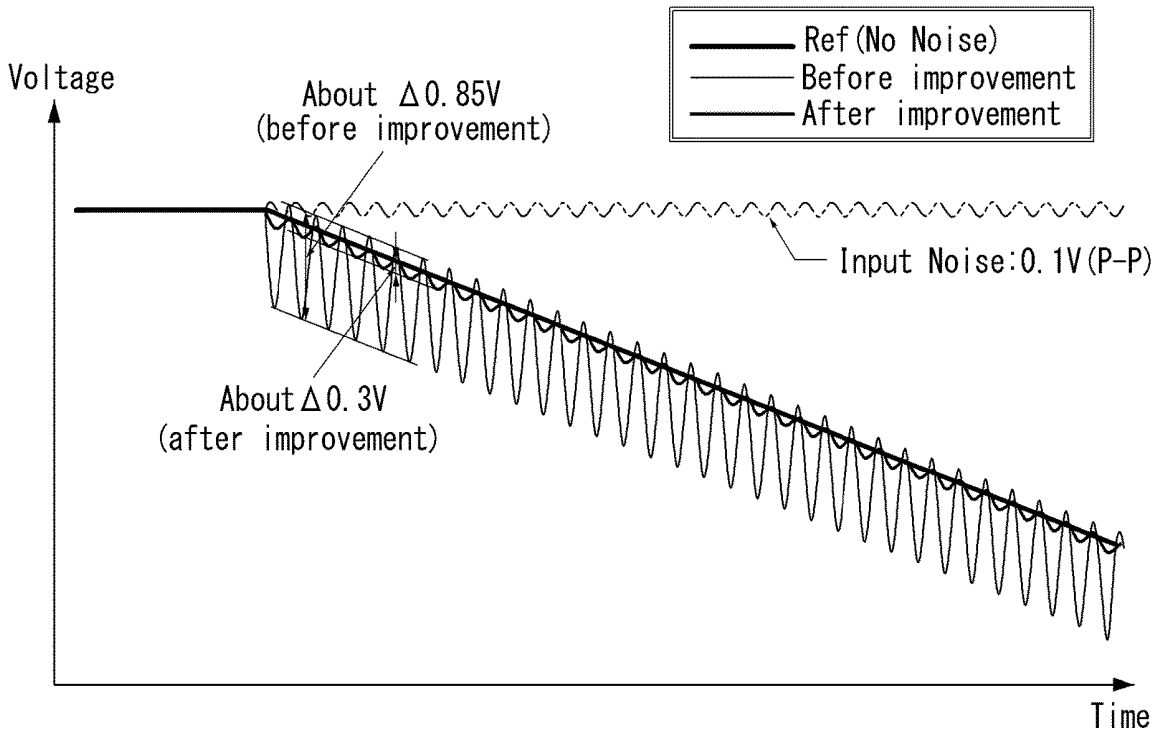
# FIG. 14


PXL
RST
CFB
SAM
1
CI-OUT
AMP
SH
ADC
CX1
AZ3
3
4
CX2
2
Vofs
AZ2
AZ1
Vref-CI

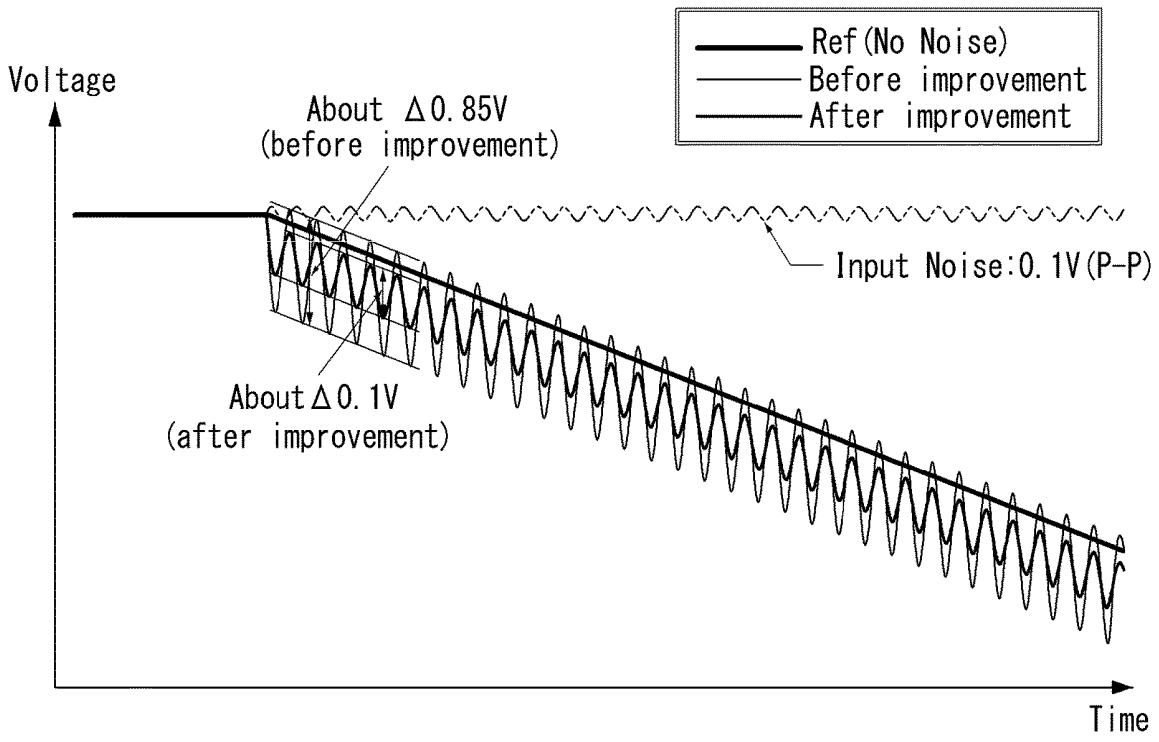
# FIG. 15


RST
PXL
CFB
Panel Noise
IPIX
SAM
1
CI-OUT
AMP
SH
ADC
CX1
AZ3
3
4
CX2
2
Panel Noise
AZ2
AZ1
Vref-CI

# FIG. 16


Ref(No Noise)
Before improvement
After improvement
Voltage
About Δ0.85V
(before improvement)
Input Noise:0.1V(P-P)
About Δ0.3V
(after improvement)
Time

# FIG. 17


Ref(No Noise)
Before improvement
After improvement
Voltage
About Δ0.85V
(before improvement)
Input Noise:0.1V(P-P)
About Δ0.1V
(after improvement)
Time

# PIXEL SENSING DEVICE AND ORGANIC LIGHT EMITTING DISPLAY DEVICE INCLUDING THE SAME

## CROSS-REFERENCE TO RELATED APPLICATION(S)

**[0001]** This application claims is based on and claims priority to Korea Patent Application No. 10-2018-0151001 filed on Nov. 29, 2018, which are incorporated herein by reference for all purposes as if fully set forth herein.

## BACKGROUND

### Technical Field

**[0002]** The present disclosure relates to a pixel sensing device and an organic light emitting display device including the same.

### Description of the Related Art

**[0003]** An organic light emitting display device of an active matrix type arranges the pixels each including an organic light emitting diode OLED a driving Thin Film Transistor TFT in a matrix form and controls the luminance of the image represented in the pixels according to the grayscale of image data. The driving TFT controls the pixel current flowing through the OLED according to the voltage applied between a gate electrode and a source electrode of the driving TFT (hereinafter, referred to as "gate-source voltage"). The amount of light emitted by the OLED and the luminance of a screen are determined according to the pixel current.

**[0004]** Since the threshold voltage and electron mobility of the driving TFT, the operating point voltage of the OLED and the like determine the driving characteristics of a pixel, the characteristics of all pixels must be substantially the same. However, due to various causes such as process properties, time varying properties and the like, the driving characteristics become different among the pixels. Such a difference in driving characteristic causes a luminance deviation, which is a limitation in displaying image as desired quality. As a method of compensating for the luminance deviation between pixels, the external compensating scheme is known which senses the driving characteristics of pixels and adjusts input image data based on the sensing results.

## BRIEF SUMMARY

**[0005]** Among the external compensating scheme, there is a method of sensing the pixel current flowing through the driving TFT using a current integrator in order to sense the driving characteristics of pixels. This method determines the change in the pixel current through the voltage difference between the reference voltage and the output voltage of the current integrator.

**[0006]** The current integrator is connected to respective pixels through sensing lines in a display panel. So, panel noise may be reflected on the pixel current sensed by the current integrator. The panel noise may be caused by various causes such as process properties, driving environment, etc., and may affect sensing channels in different sizes. Since the panel noise is amplified by an amplifier of the current integrator and distorts the output voltage of the integrator, the sensing results for a same pixel current may be different between current integrators.

**[0007]** Accordingly, in some embodiments, the present disclosure provides a pixel sensing device and the organic light emitting display device including the same which reduce or minimize the influence of the panel noise and improve sensing accuracy and sensing reliability.

**[0008]** According to one aspect of the present disclosure, a pixel sensing device includes: a current integrator connected to a pixel through a sensing line of a display panel and integrating a pixel current flowing through the pixel to generate an integrator output voltage; a sample and hold unit sampling and holding the integrator output voltage; an analog to digital converter (ADC) converting the integrator output voltage output from the sample and hold unit into a digital signal; and a first capacitor serving to reduce or minimize a distortion degree of the integrator output voltage due to panel noise mixed to the pixel current.

**[0009]** According to another aspect of the present disclosure, an organic light emitting display device includes: a display panel including a plurality of pixels; and a sensing unit for sensing driving characteristics of the pixel. The sensing unit may include a current integrator connected to the pixel through a sensing line of the display panel and integrating a pixel current flowing through the pixel to generate an integrator output voltage, a sample and hold unit sampling and holding the integrator output voltage, an analog to digital converter (ADC) converting the integrator output voltage output from the sample and hold unit into a digital signal, and a first capacitor serving to reduce or minimize a distortion degree of the integrator output voltage due to panel noise mixed to the pixel current.

## BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

**[0010]** The accompanying drawings, which are included to provide a further understanding of the present disclosure and are incorporated in and constitute a part of this specification, illustrate embodiments of the present disclosure and together with the description serve to explain the principles of the present disclosure. In the drawings:

**[0011]** FIG. **1** shows a block diagram illustrating an organic light emitting display device according to an embodiment of the present disclosure.

**[0012]** FIG. **2** shows a pixel array equipped in the display panel of FIG. **1**.

**[0013]** FIG. **3** shows the configuration of the data driving unit connected to the pixel array of FIG. **2**.

**[0014]** FIG. **4** shows an equivalent circuit of the pixel shown in FIG. **3**.

**[0015]** FIG. **5** shows another configuration of the data driving unit connected to the pixel array of FIG. **2**.

**[0016]** FIG. **6** shows an equivalent circuit of the pixel shown in FIG. **5**.

**[0017]** FIG. **7** shows the pixel sensing device according to an embodiment of the present disclosure.

**[0018]** FIG. **8** shows the waveforms of the signals applied to the pixel sensing device in FIG. **7**.

**[0019]** FIGS. **9** and **10** show the operations of the pixel sensing device in FIG. **7**.

**[0020]** FIG. **11** shows the pixel sensing device according to another embodiment of the present disclosure.

**[0021]** FIG. **12** shows the waveforms of the signals applied to the pixel sensing device in FIG. **11**.

**[0022]** FIGS. **13** to **15** show the operations of the pixel sensing device in FIG. **11**.

**[0023]** FIGS. **16** and **17** show the simulated results relating to panel noise improvement.

## DETAILED DESCRIPTION

**[0024]** The advantages and features of the present disclosure and methods of accomplishing the same may be understood more readily by reference to the following detailed descriptions of exemplary embodiments and the accompanying drawings. The present disclosure may, however, be embodied in many different forms and should not be construed as being limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure will be thorough and complete and will fully convey the concept of the present disclosure to those skilled in the art, and the present disclosure is defined by the appended claims.

**[0025]** The shapes, sizes, percentages, angles, numbers, etc., shown in the figures to describe the exemplary embodiments of the present disclosure are merely examples and not limited to those shown in the figures. Like reference numerals denote like elements throughout the specification. When the terms 'comprise', 'have', 'include' and the like are used, other parts may be added as long as the term 'only' is not used. The singular forms may be interpreted as the plural forms unless explicitly stated.

**[0026]** The elements may be interpreted to include an error margin even if not explicitly stated.

**[0027]** When the position relation between two parts is described using the terms 'on', 'over', 'connect', 'coupled', 'under', 'next to' and the like, one or more parts may be positioned between the two parts as long as the term 'immediately' or 'directly' is not used.

**[0028]** It will be understood that, although the terms first, second, etc., may be used to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, a first element referred to below may be a second element within the scope of the present disclosure.

**[0029]** In this specification, the pixel circuit and the gate driver formed on the substrate of a display panel may be implemented by a TFT of an n-type MOSFET structure, but the present disclosure is not limited thereto so the pixel circuit and the gate driver may be implemented by a TFT of a p-type MOSFET structure. The TFT or the transistor is the element of 3 electrodes including a gate, a source and a drain. The source is an electrode for supplying a carrier to the transistor. Within the TFT the carrier begins to flow from the source. The drain is an electrode from which the carrier exits the TFT. That is, the carriers in the MOSFET flow from the source to the drain. In the case of the n-type MOSFET NMOS, since the carrier is an electron, the source voltage has a voltage lower than the drain voltage so that electrons can flow from the source to the drain. In the n-type MOSFET, a current direction is from the drain to the source because electrons flow from the source to the drain. On the other hand, in the case of the p-type MOSFET PMOS, since the carrier is a hole, the source voltage has a voltage higher than the drain voltage so that holes can flow from the source to the drain. In the p-type MOSFET, a current direction is from the source to the drain because holes flow from the source to the drain. It should be noted that the source and drain of the MOSFET are not fixed. For example, the source and drain of the MOSFET may vary depending on the applied voltage. Therefore, in the description of the present disclosure, one of the source and the drain is referred to as a first electrode, and the other one of the source and the drain is referred to as a second electrode.

**[0030]** In this specification, the semiconductor layer of the TFT may be implemented by at least one of an oxide element, an amorphous silicon element, and a polysilicon element.

**[0031]** Hereinafter, various embodiments of the present disclosure will be described in detail with reference to the accompanying drawings. In describing the present disclosure, detailed descriptions of well-known functions or configurations related to the present disclosure will be omitted to avoid unnecessary obscuring the present disclosure.

**[0032]** FIG. **1** shows a block diagram illustrating an organic light emitting display device according to an embodiment of the present disclosure, and FIG. **2** shows a pixel array equipped in the display panel of FIG. **1**.

**[0033]** Referring to FIGS. **1** and **2**, the organic light emitting display device may comprise a display panel **10**, a driver IC D-IC **20**, a compensating IC **30**, a host system **40** and a storage memory **50**. The panel driving unit of the present disclosure may include a gate driving unit **15** equipped in the display panel **10** and a data driving unit **25** imbedded in the driver IC D-IC **20**. The term "unit" used herein is used broadly to indicate electronic circuits, modules of an electronic system implemented with circuitry, or the like.

**[0034]** The display panel **10** is equipped with a plurality of pixel lines PNL**1**-PNL**4**, and each pixel line is equipped with a plurality of pixels PXL and a plurality of signal lines. The pixel line in the present disclosure does not mean a physical signal line, but means a collection of the pixels PXL adjacent to each other along the direction in which a gate line extends and the signal lines. The signal lines may include the data lines **140** for supplying to the pixels PXL the data voltage for displaying VDIS and the data voltage for sensing VSEN, the reference voltage lines **150** for supplying a reference voltage VREF to the pixels PXL, the gate lines **160** for supplying gate signals to the pixels PXL and the high potential power lines PWL for supplying a high potential pixel voltage to the pixels PXL.

**[0035]** The pixels PXL in the display panel **10** are arranged in a matrix form to constituting a pixel array. Each pixel PXL included in the pixel array in FIG. **2** may be connected to one of the data lines **140**, one of the reference voltage lines **150**, one of the high potential power lines PWL and one of the gate lines **160**. Each pixel PXL included in the pixel array in FIG. **2** may be connected to a plurality of the gate lines **160**. And, a low potential pixel voltage may be supplied to each pixel PXL included in the pixel array in FIG. **2** from a power generating unit. The power generating unit may supply the low potential pixel voltage to the pixels PXL through a low potential power line or a padding unit.

**[0036]** The gate driving unit **15** may be embedded in the display panel **10**.

**[0037]** The gate driving unit **15** may include a plurality of stages connected to the gate lines **160** of the pixel array in FIG. **2**. The stages may generate the gate signals for controlling the switch elements included in the pixels PXL and supply them to the gate lines **160**.

**[0038]** The driver IC D-IC **20** may include a timing controller **21** and a data driving unit **25**. The data driving unit **25** may include a sensing unit **22** and a driving voltage generator **23**, but is not limited thereto.

**[0039]** The timing controller **21** may generate the gate timing control signals GDC for controlling the operating timings of the gate driving unit **15** and the data timing control signals DDC for controlling the operating timings of the data driving unit **25**, based on the timing signals input from the host system **40**, for example a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a dot clock signal DCLK, a data enable signal DE, and so on.

**[0040]** The data timing control signals DDC may include a source start pulse, a source sampling clock, a source output enable signal, and so on, but are not limited thereto. The source start pulse controls a data sampling start timing of the driving voltage generator **23**. The source sampling clock is a clock signal for controlling a data sampling timing based on a rising or falling edge. The source output enable signal controls an output timing of the driving voltage generator **23**.

**[0041]** The gate timing control signals GDC may include a gate start pulse, a gate shift clock, and so on, but are not limited thereto. The gate start pulse is applied to the stage of generating a first scan signal to activate the stage. The gate shift clock is commonly supplied to the stages to shift the gate start pulse.

**[0042]** The timing controller **21** may sense the driving characteristics of the pixels PXL during at least one of a power on section, vertical active intervals in each frame, a vertical blank interval in each frame and a power off section by controlling the operating timing of the panel driving unit. Here, the power on section means the period until image is displayed immediately after system power is applied, and the power off section means the period until the system power is turned off immediately after the image display is terminated. The vertical active interval is the period during which image data is written to the display panel **10** for representing screen, and the vertical blank interval is located between adjacent vertical active intervals and means the period during which the writing of the image data is suspended. The driving characteristics include the threshold voltage and electron mobility of the driving elements included in the pixels PXL.

**[0043]** The timing controller **21** may implement display driving and sense driving by controlling sense driving timing and display driving timing for pixel lines PNL**1**~PNL**4** in the display panel **10** according to a predetermined sequence.

**[0044]** The timing controller **21** may generate the timing control signals GDC and DDC for the display driving and the timing control signals GDC and DDC for the sense driving differently from each other. The sense driving means the operations which write the data voltage for sensing VSEN to the pixels PXL included in the pixel line to sense the driving characteristics of the corresponding pixels PXL, and update the compensating values for compensating for the change of the driving characteristics of the corresponding pixels PXL based on the data of the sensing results SDATA. The display driving means the operations which correct the digital image data to be input to the corresponding pixels PXL based on the updated compensating values, and apply to the corresponding pixels PXL the data voltage for displaying VDIS which corresponds to the corrected image data CDATA to display input image.

**[0045]** The driving voltage generator **23** is implemented by the digital to analog converter DAC for converting a digital signal into an analog signal. The driving voltage generator **23** generates the data voltage for sensing VSEN for the sense driving and the data voltage for displaying VDIS for the display driving and supplies them to the data lines **140**. Also, the driving voltage generator **23** generates the reference voltage VREF for the sense driving and the display driving and supplies it to the reference voltage lines **150**.

**[0046]** The data voltage for displaying VDIS may be a result of digital-to-analog conversion for the digital image data CDATA corrected in the compensating IC **30**, and the magnitude of the data voltage for displaying VDIS may vary in pixel units according to a grayscale value and a compensating value. The data voltage for sensing VSEN may be set different in units of R(red), G(Green), B(blue) and W(white) pixels in considering that the driving characteristics of the driving elements are different for respective colors.

**[0047]** The sensing unit **22** may sense the driving characteristics of the pixels PXL, for example the threshold voltage and electron mobility of a driving element, the operating point voltage of a light emitting element, and the like, to the sensing lines. The sensing lines may be implemented by using the data lines **140** or the reference voltage lines **150**. If the data lines **140** are utilized as the sensing lines, it is possible to unify a data output channel and a sensing channel, which is advantageous in reducing the number of pads of the driver IC D-IC **20**. The sensing unit **22** may be implemented as a current sensing type of directly sensing the pixel current flowing through each pixel PXL. To this end, the sensing unit **22** may include a current integrator and a capacitor for suppressing panel noise, and this will be described in detail with reference to FIG. **7**. And, the sensing unit **22** may include the current integrator, the capacitor for suppressing the panel noise and an offset removing circuit, and this will be described in detail with reference to FIG. **11**.

**[0048]** The sensing unit **22** may simultaneously or concurrently process a plurality of analog sensing values in parallel by using a plurality of ADCs, or may process the plurality of analog sensing values in a sequential manner using one ADC. The sampling rate and accuracy of the ADC are trade-offed to each other. The ADC of a parallel processing method have the advantage of increasing sensing accuracy because it can slow down a sampling rate compared to the ADC of a serial processing manner. The ADC may be implemented as the ADC of a flash type, the ADC using a tracking scheme, the ADC of a successive approximation register type, and so on. The ADC converts analog sensing values into digital sensing result data SDATA within a predetermined sensing range, and supplies the digital sensing result data SDATA to the storage memory **50** and the sensing output control unit **27**.

**[0049]** The storage memory **50** stores the digital sensing result data SDATA input from the sensing unit **22** in sense driving. The storage memory **50** may be implemented as a flash memory, but not limited thereto.

**[0050]** The compensating IC **30** may include a compensating unit **31** and a compensating memory **32**. The compensating memory **32** transmits the digital sensing result data SDATA read from the storage memory **50** to the compensating unit **31**. The compensating memory **32** may

be a random access memory RAM, for instance a double data rate synchronous dynamic RAM, but not limited thereto. The compensating unit **31** calculates a compensating offset and a compensating gain for each pixel based on the digital sensing result data SDATA read from the storage memory **50**, corrects the image data input from the host system **40** according to the compensating offset and gain, and supplies the corrected image data CDATA to the driver IC D-IC **20**.

**[0051]** FIG. **3** shows the configuration of the data driving unit connected to the pixel array of FIG. **2**. The data driving unit **25** in FIG. **3** senses the driving characteristics of the pixels PXL through the reference voltage line **150**.

**[0052]** Referring to FIG. **3**, the data driving unit **25** may be connected to the first node of the pixel PXL (e.g., the gate electrode of a driving element) through the data line **140**, and connected to the second node of the pixel PXL (e.g., the source electrode of the driving element) through the reference voltage line **150**. Since a pixel current IPIX flows through the second node of the pixel PXL, the reference voltage line **150** connected to the second node via a second switching element may be used as a sensing line.

**[0053]** The reference voltage line **150** is selectively connected to the driving voltage generator **23** and the sensing unit **22** through connecting switches SX**1** and SX**2**. The driving voltage generator **23** may comprise a first driving voltage generator DAC**1** for generating the data voltage for sensing VSEN and the data voltage for displaying VDIS, and a second driving voltage generator DAC**2** for generating the reference voltage VREF. The first connecting switch SX**1** is connected between the reference voltage line **150** and the second driving voltage generator DAC**2**, and the second connecting switch SX**2** is connected between the reference voltage line **150** and the sensing unit **22**. The first and second connecting switches SX**1** and SX**2** are selectively turned on. Only the first connecting switch SX**1** is turned on in synchronization with the timing at which the reference voltage VREF is applied to the pixel PXL, and only the second connecting switch SX**2** is turned on in synchronization with the timing at which the pixel current flowing through the pixel PXL is sensed. So, the reference voltage line **150** is selectively connected to the second driving voltage generator DAC**2** and the sensing unit **22** via the first and second connecting switches SX**1** and SX**2**.

**[0054]** FIG. **4** shows an equivalent circuit of the pixel shown in FIG. **3**.

**[0055]** Referring to the FIG. **4**, the pixel PXL utilizing the reference voltage line **150** as the sensing line comprises an OLED, a driving TFT DT, switching TFTs ST**1** and ST**2**, and a storage capacitor Cst. The driving TFT DT and the switching TFTs ST**1** and ST**2** are implemented as NMOS, but not limited thereto.

**[0056]** The OLED is an element of emitting light with the intensity corresponding to the pixel current drawn from the driving TFT DT. An anode electrode of the OLED is connected to a second node N**2** and a cathode electrode of the OLED is connected to an input terminal of a low potential voltage EVSS.

**[0057]** The driving TFT DT is a driving element for generating the pixel current according to the voltage difference between a gate electrode and a source electrode. The driving TFT DT comprises the gate electrode connected to a first node N**1**, the first electrode connected to an input terminal of a high potential voltage EVDD through the high potential power line PWL, and a second electrode connected to a second node N**2**.

**[0058]** The switching TFTs ST**1** and ST**2** are the switching elements that establish the voltage between the gate and source electrodes of the driving TFT DT and connect the second electrode of the driving TFT DT and the reference voltage line **150**.

**[0059]** The first switching TFT ST**1** is connected between the data line **140** and the first node N**1** and turned on according to a gate signal SCAN from the gate line **160**. The first switching TFT ST**1** is turned on in the program for the display driving or the sense driving. When the first switching TFT ST**1** is turned on, the data voltage for sensing VSEN or the data voltage for displaying VDIS is applied to the first node N**1**. In the first switching TFT ST**1**, a gate electrode is connected to the gate line **160**, a first electrode is connected to the data line **140** and a second electrode is connected to the first node N**1**.

**[0060]** The second switching TFT ST**2** is connected between the reference voltage line **150** and the second node N**2** and turned on according to the gate signal SCAN from the gate line **160**. The second switching TFT ST**2** is turned on in the program for the display driving or the sense driving to apply the reference voltage VREF to the second node N**2**. The second switching TFT ST**2** is also turned on in a sensing period during the sense driving, and applies the pixel current generated from the driving TFT DT to the reference voltage line **150**. In the second switching TFT ST**2**, a gate electrode is connected to the gate line **160**, a first electrode is connected to the reference voltage line **150** and a second electrode is connected to the second node N**2**.

**[0061]** The storage capacitor Cst is connected between the first node N**1** and the second node N**2** to hold the voltage between the gate and source electrodes of the driving TFT DT for a period of time.

**[0062]** FIG. **5** shows another configuration of the data driving unit connected to the pixel array of FIG. **2**. The data driving unit **25** in FIG. **5** senses the driving characteristics of the pixels PXL through the data line **140**.

**[0063]** Referring to FIG. **5**, the data driving unit **25** may be connected to the first node of the pixel PXL (e.g., the gate electrode of a driving element) through the reference voltage line **150**, and connected to the second node of the pixel PXL (e.g., the source electrode of the driving element) through the data line **140**. Since a pixel current IPIX flows through the second node of the pixel PXL, the data line **140** connected to the second node via a second switching element may be used as a sensing line.

**[0064]** The data line **140** is selectively connected to the driving voltage generator **23** and the sensing unit **22** through connecting switches SX**1** and SX**2**. The driving voltage generator **23** may comprise a first driving voltage generator DAC**1** for generating the data voltage for sensing VSEN and the data voltage for displaying VDIS, and a second driving voltage generator DAC**2** for generating the reference voltage VREF. The first connecting switch SX**1** is connected between the data line **140** and the first driving voltage generator DAC**1**, and the second connecting switch SX**2** is connected between the data line **140** and the sensing unit. The first and second connecting switches SX**1** and SX**2** are selectively turned on. Only the first connecting switch SX**1** is turned on in synchronization with the timing at which the data voltage for sensing VSEN and the data voltage for

displaying VDIS are applied to the pixel PXL, and only the second connecting switch SX**2** is turned on in synchronization with the timing at which the pixel current flowing through the pixel PXL is sensed. So, the data line **140** is selectively connected to the first driving voltage generator DAC**1** and the sensing unit **22** via the first and second connecting switches SX**1** and SX**2**.

**[0065]** FIG. **6** shows an equivalent circuit of the pixel shown in FIG. **5**.

**[0066]** Referring to the FIG. **6**, the pixel PXL utilizing the data line **140** as the sensing line comprises an OLED, a driving TFT DT, switching TFTs ST**1** and ST**2**, and a storage capacitor Cst. The driving TFT DT and the switching TFTs ST**1** and ST**2** are implemented as NMOS, but not limited thereto.

**[0067]** The OLED is an element of emitting light with the intensity corresponding to the pixel current drawn from the driving TFT DT. An anode electrode of the OLED is connected to a second node N**2** and a cathode electrode of the OLED is connected to an input terminal of the low potential voltage EVSS.

**[0068]** The driving TFT DT is a driving element for generating the pixel current according to the voltage difference between a gate electrode and a source electrode. The driving TFT DT comprises the gate electrode connected to a first node N**1**, a first electrode connected to an input terminal of the high potential voltage EVDD through the high potential power line PWL, and a second electrode connected to a second node N**2**.

**[0069]** The switching TFTs ST**1** and ST**2** are the switching elements that establish the voltage between the gate and source electrodes of the driving TFT DT and connect the second electrode of the driving TFT DT and the data line **140**.

**[0070]** The first switching TFT ST**1** is connected between the reference voltage line **150** and the first node N**1** and turned on according to the gate signal SCAN from the gate line **160**. The first switching TFT ST**1** is turned on in the program for the display driving or the sense driving. When the first switching TFT ST**1** is turned on, the reference voltage VREF is applied to the first node N**1**. In the first switching TFT ST**1**, a gate electrode is connected to the gate line **160**, a first electrode is connected to the reference voltage line **150** and a second electrode is connected to the first node N**1**.

**[0071]** The second switching TFT ST**2** is connected between the data line **140** and the second node N**2** and turned on according to the gate signal SCAN from the gate line **160**. The second switching TFT ST**2** is turned on in the program for the display driving or the sense driving to apply the data voltage for sensing VSEN or the data voltage for displaying VDIS to the second node N**2**. The second switching TFT ST**2** is also turned on in a sensing period during the sense driving, and applies the pixel current generated from the driving TFT DT to the data line **140**. In the second switching TFT ST**2**, a gate electrode is connected to the gate line **160**, a first electrode is connected to the data line **140** and a second electrode is connected to the second node N**2**.

**[0072]** The storage capacitor Cst is connected between the first node N**1** and the second node N**2** to hold the voltage between the gate and source electrodes of the driving TFT DT for a period of time.

**[0073]** FIG. **7** shows the pixel sensing device according to an embodiment of the present disclosure. The pixel sensing device in FIG. **7** includes the sensing unit **22** in FIG. **1**.

**[0074]** Referring to FIG. **7**, the sensing unit **22** may include a current integrator CI, a sample and hold unit SH, an ADC and a first capacitor CX**1**.

**[0075]** The current integrator CI is connected to a pixel PXL through a sensing line of the display panel **10**. The current integrator CI integrates the pixel current IPIX flowing through the pixel PXL to generate an integrator output voltage CI-OUT that varies from an integrator reference voltage Vref-CI.

**[0076]** The current integrator CI comprises an amplifier AMP, an integrating capacitor CFB and a reset switch RST. The amplifier AMP is equipped with a first input terminal to receive the pixel current IPIX through a first node (1) connected to the sensing line, a second input terminal to receive the integrator reference voltage Vref-CI through a second node (2) and an output terminal to output the integrator output voltage CI-OUT corresponding to a result of integrating the pixel current IPIX to a third node (3). The integrating capacitor CFB is connected between the first node (1) and the third node (3), that is, the integrating capacitor CFB is connected between the first input terminal and the output terminal of the amplifier AMP. The reset switch RST is further connected between the first input terminal and the output terminal of the amplifier AMP in parallel with the integrating capacitor CFB.

**[0077]** The amplifier AMP may be implemented as a negative type or positive type. In the amplifier AMP of the negative type as shown in FIG. **7**, the first input terminal is an inverting input terminal (−) of the amplifier AMP and the second input terminal is an non-inverting input terminal (+) of the amplifier AMP. In this negative-typed amplifier AMP, the integrator output voltage CI-OUT gradually decreases from the integrator reference voltage Vref-CI as the pixel current IPIX is accumulated in the integrating capacitor CFB. The falling slope of the integrator output voltage CI-OUT is proportional to the magnitude of the pixel current IPIX.

**[0078]** On the other hand, in amplifier AMP of the positive type, the first input terminal is an non-inverting input terminal (+) of the amplifier AMP and the second input terminal is an inverting input terminal (−) of the amplifier AMP. In this positive-typed amplifier AMP, the integrator output voltage CI-OUT gradually increases from the integrator reference voltage Vref-CI as the pixel current IPIX is accumulated in the integrating capacitor CFB. The rising slope of the integrator output voltage CI-OUT is proportional to the magnitude of the pixel current IPIX.

**[0079]** The idea of the present disclosure may be applied to the negative-typed amplifier and also applied to the positive-typed amplifier. In the embodiment of the present disclosure, the negative-typed amplifier will be mainly described for the sake of convenience.

**[0080]** The sample and hold unit SH samples and holds the integrator output voltage CI-OUT and then outputs it to the ADC. The sample and hold unit SH may comprise a sampling capacitor, a sampling switch and a holding switch operating according to a sampling signal SAM, but is not limited thereto.

**[0081]** The ADC converts an analog signal (that is the integrator output voltage) into a digital signal (that is digital sensing result data) within a predetermined sensing range.

**[0082]** The first capacitor CX**1** serves to reduce or minimize the distortion degree of the integrator output voltage CI-OUT due to panel noise. The first capacitor CX**1** is connected between the first node (1) and the second node (2) to couple the first input terminal (−) and the second input terminal (+) of the amplifier AMP. The first capacitor CX**1** allows the panel noise which is mixed to the pixel current IPIX to be commonly applied to both the input terminals (+) and (−) of the amplifier AMP. The panel noise mixed to the pixel current IPIX is applied to the first input terminal (−) of the amplifier AMP and also applied to the second input terminal (+) of the amplifier AMP through the first capacitor CX**1**. So, the panel noise applied to both the input terminals (+) and (−) of the amplifier AMP may be canceled inside the amplifier AMP to be reduced or minimized.

**[0083]** The larger the capacitance of the first capacitor CX**1**, the smaller the amount of the panel noise that is mixed into the integrator output voltage CI-OUT. This is because the magnitude of the panel noise applied to the first input terminal (−) of the amplifier AMP becomes similar to that of the panel noise applied to the second input terminal (+) of the amplifier AMP as the capacitance of the first capacitor CX**1** becomes larger. Ideally, when the magnitudes of the panel noise applied to both the input terminals (+) and (−) of the amplifier AMP are same, the panel noise to be mixed into the integrator output voltage CI-OUT may be completely canceled.

**[0084]** FIG. **8** shows the waveforms of the signals applied to the pixel sensing device in FIG. **7**, and FIGS. **9** and **10** show the operations of the pixel sensing device in FIG. **7**.

**[0085]** Referring to FIG. **8**, the sense driving according to an embodiment of the present disclosure may be implemented to include an initializing period ① and a sensing period ②.

**[0086]** Referring to FIGS. **8** and **9**, in the initializing period ①, the reset switch RST is turned on. If the reset switch RST is turned on, the sensing line as well as the first to third nodes (1), (2) and (3) are initialized to the integrator reference voltage Vref-CI. So, in the initializing period ① the integrator output voltage CI-OUT becomes the integrator reference voltage Vref-CI.

**[0087]** Referring to FIGS. **8** and **10**, in the sensing period ②, the reset switch RST is turned off and the charges according to the pixel current IPIX input through the sensing line and the first node (1) are accumulated in the integrating capacitor CFB. As the charges according to the pixel current IPX are accumulated in the integrating capacitor CFB, the integrator output voltage CI-OUT is gradually lowered from the integrator reference voltage Vref-CI.

**[0088]** In the sensing period ②, since the panel noise mixed into the pixel current IPIX is applied to both the input terminals (+) and (−) of the amplifier AMP through the first capacitor CX**1** and canceled inside the amplifier AMP, the panel noise to be mixed into the integrator output voltage CI-OUT is reduced or minimized.

**[0089]** In the sensing period ②, the sample and hold unit SH samples the integrator output voltage CI-OUT during the sampling signal SAM is of on level.

**[0090]** FIG. **11** shows the pixel sensing device according to another embodiment of the present disclosure. The pixel sensing device in FIG. **11** may further improve sensing accuracy because it can further remove an amplifier offset as compared to that of FIG. **7**.

**[0091]** Referring to FIG. **11**, the sensing unit **22** may comprise a current integrator CI, a sample and hold unit SH, an ADC and a first capacitor CXI, and may further comprise an offset cancelling unit CAZ.

**[0092]** The current integrator CI is connected to a pixel PXL through a sensing line of the display panel **10**. The current integrator CI integrates the pixel current IPIX flowing through the pixel PXL to generate an integrator output voltage CI-OUT that varies from an integrator reference voltage Vref-CI.

**[0093]** The current integrator CI comprises an amplifier AMP, an integrating capacitor CFB and a reset switch RST. The amplifier AMP is equipped with a first input terminal to receive the pixel current IPIX through a first node (1) connected to the sensing line, a second input terminal to receive the integrator reference voltage Vref-CI through a second node (2) and an output terminal to output the integrator output voltage CI-OUT corresponding to a result of integrating the pixel current IPIX to a third node (3). The integrating capacitor CFB is connected between the first node (1) and the third node (3), that is, the integrating capacitor CFB is connected between the first input terminal and the output terminal of the amplifier AMP. The reset switch RST is further connected between the first input terminal and the output terminal of the amplifier AMP in parallel with the integrating capacitor CFB.

**[0094]** The sample and hold unit SH samples and holds the integrator output voltage CI-OUT and then outputs it to the ADC. The sample and hold unit SH may comprise a sampling capacitor, a sampling switch and a holding switch operating according to a sampling signal SAM, but is not limited thereto.

**[0095]** The ADC converts an analog signal (that is the integrator output voltage) into a digital signal (that is digital sensing result data) within a predetermined sensing range.

**[0096]** The first capacitor CX**1** serves to reduce or minimize the distortion degree of the integrator output voltage CI-OUT due to panel noise, together with a second capacitor CX**2** included in the offset cancelling unit CAZ. The first capacitor CX**1** and the second capacitor CX**2** are connected between the first node (1) and the second node (2) to couple the first input terminal (−) and the second input terminal (+) of the amplifier AMP.

**[0097]** The offset cancelling unit CAZ is connected to the input terminal of the integrator reference voltage Vref-CI, the first node (1) and the second node (2), and applies to the amplifier AMP a correcting reference voltage which can cancel an offset of the amplifier AMP through the second node (2). The offset cancelling unit CAZ includes the second capacitor CX**2** and first to third switches AZ**1**, AZ**2** and AZ**3**.

**[0098]** The second capacitor CX**2** is equipped with one electrode connected to the second node (2) and the other electrode connected to the first capacitor CX**1** through a fourth node (4). Between the first node (1) and the second node (2), the second capacitor CX**2** is connected in series with the first capacitor CX**1**. The second capacitor CX**2** is connected to the first capacitor CX**1** through the fourth node (4).

**[0099]** The first and second capacitors CX**1** and CX**2** allows the panel noise which is mixed to the pixel current IPIX to be commonly applied to both the input terminals (+) and (−) of the amplifier AMP. The panel noise mixed to the pixel current IPIX is applied to the first input terminal (−) of the amplifier AMP and also applied to the second input

terminal (+) of the amplifier AMP through the first and second capacitors CX1 and CX2. So, the panel noise applied to both the input terminals (+) and (−) of the amplifier AMP may be canceled inside the amplifier AMP to be reduced or minimized.

**[0100]** The larger the capacitances of the first and second capacitors CX1 and CX2, the smaller the amount of the panel noise that is mixed into the integrator output voltage CI-OUT. This is because the magnitude of the panel noise applied to the first input terminal (−) of the amplifier AMP becomes similar to that of the panel noise applied to the second input terminal (+) of the amplifier AMP as the capacitance of the first and second capacitors CX1 and CX2 becomes larger. Ideally, when the magnitudes of the panel noise applied to both the input terminals (+) and (−) of the amplifier AMP are same, the panel noise to be mixed into the integrator output voltage CI-OUT may be completely canceled.

**[0101]** Meanwhile, the first switch AZ1 is connected between the second node (2) and the input terminal of the integrator reference voltage Vref-CI. The second switch AZ2 is connected between the fourth node (4) and the input terminal of the integrator reference voltage Vref-CI. The third switch AZ3 is connected between the first node (1) and the fourth node (4). By the switching actions of the first to third switches AZ1, AZ2 and AZ3 and the coupling effect of the second capacitor CX2, the correcting reference voltage which may cancel the offset of the amplifier AMP may be applied to the amplifier AMP through the second node (2).

**[0102]** FIG. **12** shows the waveforms of the signals applied to the pixel sensing device in FIG. **11**, and FIGS. **13** to **15** show the operations of the pixel sensing device in FIG. **11**.

**[0103]** Referring to FIG. **12**, the sense driving according to another embodiment of the present disclosure may be implemented to include an offset detecting period ①, an initializing period ②, and a sensing period ③.

**[0104]** Referring to FIGS. **12** and **13**, in the offset detecting period ①, the first and third switches AZ1 and AZ3 and the reset switch RST are turned on and the second switch AZ2 is turned off. If first and third switches AZ1 and AZ3 and the reset switch RST is turned on, the integrator reference voltage Vref-CI is applied to the second node (2), and a first integrator reference voltage (Vref-CI+Vofs) to which the offset Vofs of the amplifier AMP is added is applied to the first, third and fourth node (1), (3) and (4) and the sensing line. So, in the offset detecting period ①, the offset Vofs of the amplifier AMP is detected to be stored in the second capacitor CX2.

**[0105]** Referring to FIGS. **12** and **14**, in the initializing period ①, the first switch AZ1 and the third switch AZ3 are turned off, and the reset switch RST and the second switch AZ2 are turned on. If the reset switch RST is turned on, the voltage of the fourth node (4) changes from a first integrator reference voltage (Vref-CI+Vofs) to the integrator reference voltage Vref-CI. Since the first switch AZ1 is turned off at this time, the second node (2) is floated, and the voltage of the second node (2) changes from the integrator reference voltage Vref-CI to a second integrator reference voltage (Vref-CI−Vofs) due to the coupling action of the second capacitor CX2. The offset Vofs of the amplifier AMP is canceled by the second integrator reference voltage (Vref-CI−Vofs) applied through the second node (2). And, since the reset switch RST is of a turn-on state at this time, the voltages of the first node (1), the third node (3) and the sensing line change from the first integrator reference voltage (Vref-CI+Vofs) to the integrator reference voltage Vref-CI. That is, in the initializing period ②, the voltages of the first node (1) and the third node (3) is initialized to the integrator reference voltage Vref-CI while the offset Vofs of the amplifier AMP is removed.

**[0106]** Referring to FIGS. **12** and **15**, in the sensing period ③, the first switch AZ1, the second switch AZ2, the third switch AZ3 and the reset switch RST are turned off, the charges according to the pixel current IPIX input through the sensing line and the first node (1) are accumulated in the integrating capacitor CFB. As the charges according to the pixel current IPX are accumulated in the integrating capacitor CFB, the integrator output voltage CI-OUT is gradually lowered from the integrator reference voltage Vref-CI.

**[0107]** In the sensing period ③, since the panel noise mixed into the pixel current IPIX is applied to both the input terminals (+) and (−) of the amplifier AMP by the first and second capacitors CX1 and CX2 and canceled inside the amplifier AMP, the panel noise to be mixed into the integrator output voltage CI-OUT is reduced or minimized.

**[0108]** In the sensing period ③, the offset of amplifier AMP is removed from the integrator output voltage CI-OUT, so the distortion of the integrator output voltage CI-OUT due to the offset Vofs of the amplifier AMP is remarkably reduced.

**[0109]** In the sensing period ③, the sample and hold unit SH samples the integrator output voltage CI-OUT during the sampling signal SAM is of on level.

**[0110]** FIGS. **16** and **17** show the simulated results relating to panel noise improvement.

**[0111]** As known from the simulated results of FIGS. **16** and **17**, if the pixel sensing device applies the panel noise mixed to the pixel current IPIX to both the input terminals (+) and (−) through the first capacitor CX1 or through the first and second capacitors CX1 and CX2 and integrates the pixel current IPIX, it may remarkably reduce the magnitude of the panel noise to be mixed to the integrator output voltage CI-OUT.

**[0112]** Referring to FIG. **16**, when setting the capacitance of the first capacitor CX1 or the combined capacitance of the first capacitor CX1 and the second capacitor CX2 to be 10 pF, the magnitude of the panel noise becomes about 0.3V, which is a significant improvement over 0.85V before improvement (capacitorless).

**[0113]** Referring to FIG. **17**, when increasing the capacitance of the first capacitor CX1 or the combined capacitance of the first capacitor CX1 and the second capacitor CX2 to be 50 pF, the magnitude of the panel noise becomes about 0.1V, which is a remarkable improvement over 0.85V before improvement (capacitorless).

**[0114]** Referring to FIGS. **16** and **17**, it can be known that the larger the capacitance of the first capacitor CX1 (or the combined capacitance of the first capacitor CX1 and the second capacitor CX2), the less the amount of the panel noise to be mixed to the integrator output voltage CI-OUT.

**[0115]** As described above, in the present disclosure, the capacitor for suppressing the panel noise is equipped in the sensing unit together with the current integrator, thereby minimizing the amount of panel noise mixed to the integrator output voltage, thereby improving the accuracy and reliability of sensing.

**[0116]** And, by further comprising the offset cancelling circuit in the sensing unit, the present disclosure may reduce or minimize the distortion of the integrator output voltage which occurs due to the offset of the integrating amplifier to further improve the accuracy and reliability of sensing.

**[0117]** Throughout the description, it should be understood by those skilled in the art that various changes and modifications are possible without departing from the technical principles of the present disclosure. Therefore, the technical scope of the present disclosure is not limited to the detailed descriptions in this specification but should be defined by the scope of the appended claims.

**[0118]** The various embodiments described above can be combined to provide further embodiments. All of the U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet are incorporated herein by reference, in their entirety. Aspects of the embodiments can be modified, if necessary to employ concepts of the various patents, applications and publications to provide yet further embodiments.

**[0119]** These and other changes can be made to the embodiments in light of the above-detailed description. In general, in the following claims, the terms used should not be construed to limit the claims to the specific embodiments disclosed in the specification and the claims, but should be construed to include all possible embodiments along with the full scope of equivalents to which such claims are entitled. Accordingly, the claims are not limited by the disclosure.

**1**. A pixel sensing device, comprising:
- a current integrator connected to a pixel through a sensing line of a display panel, the current integrator integrating a pixel current flowing through the pixel to generate an integrator output voltage, the pixel current including panel noise;
- a sample and hold unit sampling and holding the integrator output voltage;
- an analog to digital converter converting the integrator output voltage output from the sample and hold unit into a digital signal; and
- a first capacitor coupled to the current integrator serving to reduce a distortion degree of the integrator output voltage due to the panel noise mixed to the pixel current.

**2**. The pixel sensing device according to claim **1**, wherein the current integrator comprises:
- an amplifier having a first input terminal connected to the sensing line for receiving the pixel current, a second input terminal for receiving an integrator reference voltage, and an output terminal for outputting the integrator output voltage that varies from the integrator reference voltage;
- an integrating capacitor connected between the first input terminal and the output terminal of the amplifier; and
- a reset switch connected between the first input terminal and the output terminal of the amplifier in parallel with the integrating capacitor,
- wherein the first capacitor couples the first input terminal and the second input terminal of the amplifier.

**3**. The pixel sensing device according to claim **1**, wherein the panel noise mixed to the pixel current is applied to the first input terminal of the amplifier and applied to the second input terminal of the amplifier through the first capacitor, such that the panel noise is canceled inside the amplifier to be reduced, in a sensing period in which charges of the pixel current are accumulated in the integrating capacitor.

**4**. The pixel sensing device according to claim **2**, wherein the first capacitor is connected between the sensing line and the second input terminal of the amplifier.

**5**. The pixel sensing device according to claim **2**, further comprising:
- an offset cancelling unit serving to remove an offset of the integrating amplifier from the integrator output voltage.

**6**. The pixel sensing device according to claim **5**, wherein the offset cancelling unit comprises:
- a second capacitor connected between the first capacitor and the second input terminal of the amplifier and coupling the first input terminal and the second input terminal of the amplifier together with the first capacitor;
- a first switch connected between the second input terminal of the amplifier and an input terminal of the integrator reference voltage;
- a second switch connected between the input terminal of the integrator reference voltage and a node between the first capacitor and the second capacitor; and
- a third switch connected between the first input terminal of the amplifier and the node between the first capacitor and the second capacitor.

**7**. The pixel sensing device according to claim **6**, wherein the first switch, the third and the reset switch are turned on and the second switch is turned off to store the offset of the amplifier in the second capacitor, in an offset detecting period.

**8**. The pixel sensing device according to claim **6**, wherein the first switch and the third switch are turned off and the reset switch and the second switch are turned on to float the second input terminal of the amplifier and initialize voltages of the first input terminal and the output terminal of the amplifier to the integrator reference voltage, in an initializing period.

**9**. The pixel sensing device according to claim **6**, wherein the first switch, the second switch, the third switch and the reset switch are turned off to accumulate charges of the pixel current in the integrating capacitor and generate the integrator output voltage from which the offset of the amplifier is removed, in a sensing period.

**10**. The pixel sensing device according to claim **9**, wherein the panel noise mixed to the pixel current is applied to the first input terminal of the amplifier and applied to the second input terminal of the amplifier through the first capacitor and the second capacitor, such that the panel noise is canceled inside the amplifier to be reduced, in the sensing period.

**11**. An organic light emitting display device, comprising:
- a display panel including a plurality of pixels; and
- a sensing unit for sensing driving characteristics of the pixel, the sensing unit including:
  - a current integrator connected to the pixel through a sensing line of the display panel, the current integrator integrating a pixel current flowing through the pixel to generate an integrator output voltage, the pixel current including panel noise;
  - a sample and hold unit sampling and holding the integrator output voltage;

an analog to digital converter converting the integrator output voltage output from the sample and hold unit into a digital signal; and

a first capacitor adjacent to the current integrator serving to reduce a distortion degree of the integrator output voltage due to the panel noise mixed to the pixel current.

**12**. The organic light emitting display device according to claim **11**, further comprising:

a driving voltage generator for generating data voltage for sensing for sense driving and data voltage for displaying for display driving and supplying them to a data line of the display panel, and generating a reference voltage for the sense driving and the display driving and supplying it to a reference voltage line of the display panel.

**13**. The organic light emitting display device according to claim **12**, wherein the data line is used as the sensing line.

**14**. The organic light emitting display device according to claim **12**, wherein the reference voltage line is used as the sensing line.

**15**. The organic light emitting display device according to claim **11**, further comprising:

a timing controller for controlling sense driving timing and display driving timing of the display panel,

wherein the sensing unit senses the driving characteristics of the pixel during at least one of a power on section, a vertical active interval in each frame, a vertical blank interval in each frame and a power off section under control of the timing controller.

**16**. The organic light emitting display device according to claim **12**, further comprising:

a compensating unit for calculating a compensating value for compensating for a change of the driving characteristics of the pixel based on a digital sensing result data from the sensing unit, correcting an image data input from a host system according to the compensating value, and supplying the corrected image data to the driving voltage generator,

wherein the driving voltage generator generates the data voltage for displaying based on the corrected image data.

**17**. The organic light emitting display device according to claim **12**, wherein the sensing unit and the driving voltage generator are included in a data driving unit.

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摘要(译)

本公开涉及一种像素感测装置和包括该像素感测装置的有机发光显示装置，该像素感测装置和有机发光显示装置减小或最小化面板噪声的影响并提高感测精度和感测可靠性。 像素感测装置包括电流积分器，该电流积分器通过显示面板的感测线连接到像素，并且积分流过像素的像素电流以产生积分器输出电压；以及 采样保持单元采样并保持积分器的输出电压； 模数转换器（ADC），将采样保持单元输出的积分器输出电压转换为数字信号； 第一电容器，用于减小或最小化由于混合到像素电流的面板噪声引起的积分器输出电压的失真度。